

Appl. No. 10/065, 011
Amdt dated July 06, 2004
Reply to Office Action of April 07, 2004

REMARKS/ARGUMENTS

Status of Application

Claims 1-20 are pending in the subject application. Claim 1 is rejected under 35 USC § 102. Claims 2-20 are objected as being dependent upon a rejected base claim.

Objection to the Drawings

Figure 1 has been objected to by the Examiner. Specifically, Figure 1 should be designated by a legend "Prior Art" because only that which is old is illustrated. Applicants, in response, have amended Figure 1 as suggested by the Examiner. Applicants therefore submit that the objection to the drawings has been traversed.

Rejections under 35 USC § 102

Claim 1 is rejected under 35 USC § 102(b) as being anticipated by Casper (U.S. Patent No. 6,141,270). Applicants respectfully disagree.

Claim 1 has been amended to more clearly recite the invention. As amended, claim 1 recites an integrated circuit having a sense amplifier and first and second bitlines coupled thereto. A plurality of memory cells are coupled to the sense amplifiers. During a memory access, a selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier. A test circuit is coupled to the bitlines. The test circuit, when activated, varies the magnitude of the differential read signal by changing the capacitance of at least one of the bitlines.

Casper describes a method for testing cell margin for a memory cell in a dynamic cell plate sensing array architecture. The method includes the use of isolation device to selectively

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isolate either a digit line or a plate line associated with the accessed memory cell while the other line is coupled to the sense amplifier. The line coupled to the sense amplifier swings due to charge transfer from the selected memory cell signal while the other line is maintained at a reference potential. Varying the magnitude of the differential read signal using a test circuit to change the capacitance of at least one of the bitlines, as presently recited in claim 1, is nowhere taught or suggested by Casper. Applicants submit that claim 1 is patentable over Casper. Since new claims 21-23 are directly or indirectly dependent on claim 1 and new claim 25 recite a method of operating an integrated circuit, which like the integrated circuit of claim 1, varies the magnitude of the differential read signal by changing the capacitance of at least one of the bitlines, these claims are also patentable over Casper. Therefore, Applicants respectfully request withdrawal of the rejection based on 35 USC § 102(b).

Allowable Subject Matter

Claims 2-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Applicants have amended claims 2 and 3 to be in independent form which include all of the limitations of the base claim. As for newly added claim 24, it includes all the limitations of claim 1 and claim 4. Therefore, claims 2-3 and 24 are now allowable. Since claims 4-20 are directly or indirectly dependent on claim 2, these claims are also allowable.

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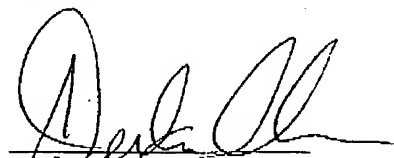
Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: July 06, 2004

Respectfully submitted,



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